A 1MHz-64MHz Active RC TI-LPF with Variable Gain for SDR Receiver in 65-nm CMOS

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Abstract. This paper reports an active RC trans-impedance low pass filter (TI-LPF) with variable gain and bandwidth that can be used in 200MHz to 6GHz zero-IF software-defined radio (SDR) receivers. This paper not only incorporates a single pole Butterworth TI-LPF, but also includes voltage detector for auto-gain control (AGC) systems. Influence of finite gain amplifier and the architecture of this zero-IF SDR receiver, which uses a 65-nm CMOS process, are introduced in this paper as well. Using 65nm CMOS process, this TI-LPF exhibits 64x bandwidth tunability (1MHz to 64MHz), 3 stages of trans-impedance gain of 71.2dBΩ, 67.6dBΩ and 65.1dBΩ, a static power dissipation less than 6.002mW, and a total summarized noise less than 5.969 x $10^{-15}V^2$.

1. Introduction

Since the information technology revolution, the design of RF analog circuits is always depended on manual design. But manufacturers of analog devices are hard to keep up to wireless bands and services' development, where new service emerges every six months [1]. As first proposed by Mitola [2] in 1992, software-defined radio (SDR) has been developed for more than 20 years [4, 5]. In this paper, part of the a zero-IF SDR receiver's baseband filters is reported. The trans-impedance low pass filter (TI-LPF) with variable gain and bandwidth is designed based on the trans-impedance amplifier (TIA) with a feedback which measures the input current, which can be used in multi- modulation highly linear wideband receivers. This design of TI-LPF is used in a 200MHz to 6GHz zero-IF SDR receiver.

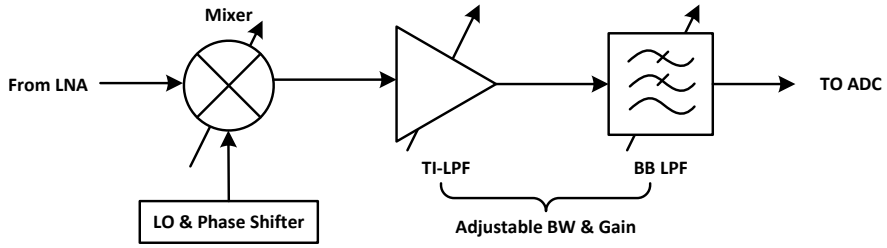


Fig. 1 Application diagram of the TI-LPF

Application diagram of this TI-LPF is shown in Fig. 1, using in zero-IF system. With a former stage of current mixer and a later stage of baseband (BB) low pass filter (LPF), TI-LPF converts current signal to voltage signal, and provides preliminary filtering of signal. To support as many communication protocols as possible, such as GSM, LTE, CDMA, WLAN, Bluetooth, etc. in 200MHz to 6GHz, this design exhibits 1MHz to 64MHz bandwidth tunability. Consider auto-gain control (AGC) for the system, this module provides 3 stages of trans-impedance gain of 71.2dBΩ, 67.6dBΩ and 65.1dBΩ.

2. Front-end of SDR Receiver

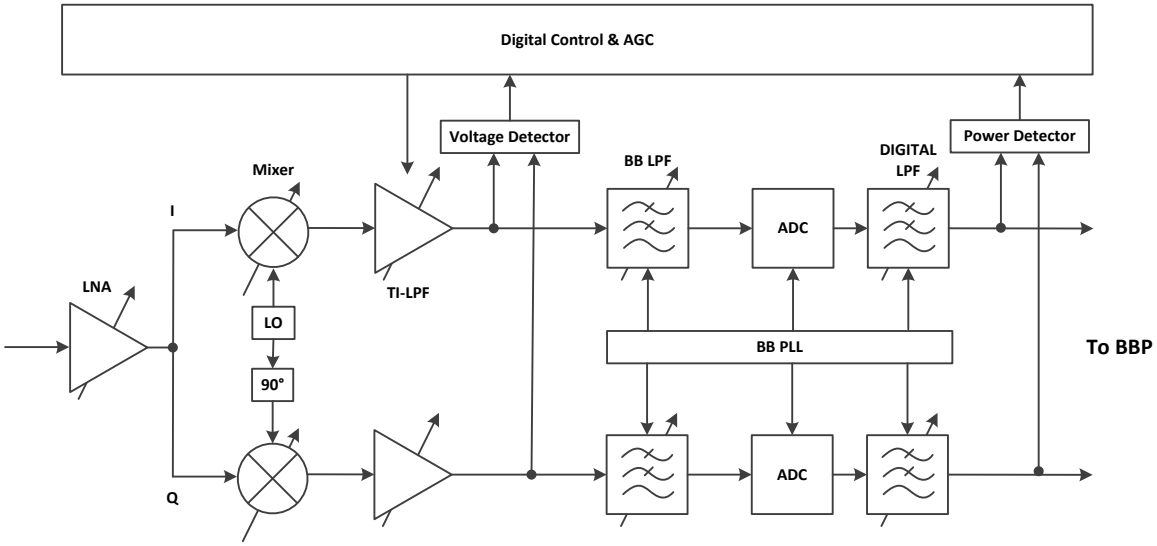


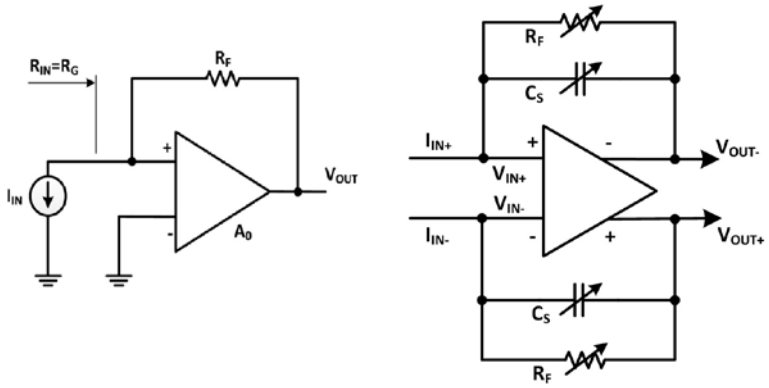
Fig. 2 Architecture of 200MHz to 6GHz zero-IF SDR receiver

The concept of SDR comes from military applications, where a transceiver should modulate and demodulate a wide enough bandwidth at the same time [3]. To cover communication protocols of 200MHz to 6GHz, zero-IF architecture is used in the SDR front-end (Fig. 2). The LNA and current mixer are both wideband modules. RF local oscillator (LO) provides 200MHz to 6GHz frequency for quadrature down-conversion mixer. TI-LPF and BB LPF provides 200kHz to 40MHz adjustable -3dB corner frequency for anti-aliasing. On the other hand, so many communication services mean this receiver need a high dynamic range ADC, using a 4-stage delta-sigma structure. Digital LPF provides filtering and decimation to reduce sampling frequency to Nyquist frequency.

The difficulty of wideband zero-IF receivers for SDR lies in wideband Mixer, wide tuning range of baseband, DC offset calibration and AGC of receive chain. Passive mixer is used because of the high linearity, so that the first stage of baseband filters (BBF) should be a trans-impedance stage. In next few chapters, more details of TI-LPF and voltage detector will be given.

3. Influence of Finite Gain Amp

The basic structure of transimpedance amplifier (TIA) with a feedback which measures the input current is shown in Fig. 3 (a). This structure is introduced in [8] in detail. By using this structure after a passive current mixer in receive chain, we designed TI-LPF schematic as Fig. 3 (b).



(a) (b)

Fig. 3 Architecture of 200MHz to 6GHz zero-IF SDR receiver

For infinite gain amplifier, the s domain transfer function of V_{out+}-Vout- and I_{in+}-I_{in-} can be expressed as

$$T(s) = \frac{R_F}{1 + sR_F C_S} \tag{1}$$

where RF is the feedback resister array, CS is the feedback capacitor array. The transimpedance at low-frequency equals to RF. 3 different trans-impedance gain lead to a 3 resisters' (3.6kΩ, 2.4kΩ and 1.8kΩ) array RF. Time constant τ = RFCS. Thus, CS can be expressed as

$$C_S = \frac{1}{2\pi f R_F} \tag{2}$$

where f is the frequency of input signal. We note that CS is in inverse proportion to f. To get a equal step for variable -3dB bandwidth, the capacitor should be designed in inverse radio.

However, 65nm CMOS process can not provide high gain (such 80dB) for amplifiers. For this reason, we should first analyse the influence of finite gain amplifier. For a finite gain amplifier, which gain can expressed as

$$A_0(\omega) = \frac{A}{1 + j\omega/\omega_H} \tag{3}$$

where A is the low-frequency gain and ωH is the -3dB bandwidth of the finite gain amplifier. By using Kirchhoff's law, we can get the jω function with $A_0(\omega)$ as

$$T(j\omega) = Z_F \frac{A_0(\omega)}{A_0(\omega) + 1} \tag{4}$$

where trans-impedance $Z_F = T(s)$. Transform the upper expression as

$$T(j\omega) = Z_F \frac{1}{1 + \frac{1}{A} + j\frac{\omega}{A\omega_H}} \tag{5}$$

where $A\omega_H$ = GBW. Ignoring 1/A in (5), we can get a conclusion that when GBW equals signal bandwidth, the trans-impedance gain will decrease by 3dB at ω. It means that the GBW of finite gain Amp must be designed bigger than signal bandwidth. Observe that when GBW is ten times than signal bandwidth, trans-impedance gain will decrease 0.05dB at ω. Thus, when design this TI-LPF, we try our best to make the GBW of Amp to be bigger than 10 times of ω for fear of the decrease of trans-impedance caused by finite gain.

4. Design of Circuit Schematics

4.1 Amplifier for TI-LPF

The amplifier circuit schematics of the TI-LPF reported by this paper is shown in Fig. 4. The structure of Amp is designed for low-voltage, for 65nm CMOS process's 1.2V supply voltage. The 1st stage is a differential pair amplifier with current-source load. The 2nd stage is a common-source amplifier. The BIAS circuit in Fig. 4 provides a floating bias voltage, which increase stability of the Amp, by a parallel differential inputs structure.

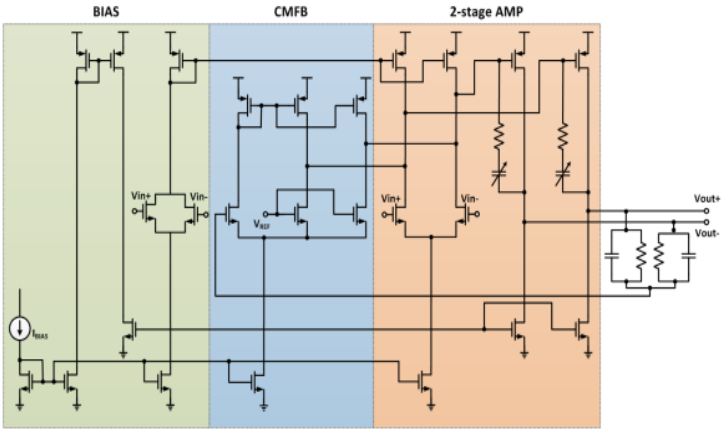


Fig. 4 Circuit schematics of the TI-LPF's amplifier

Referring to the contents of the previous chapter, the amplifier's GBW is designed as 10 times of signal bandwidth. While signal bandwidth of this TI-LPF is adjustable from 1MHz to 64MHz, so the GBW of this amplifier is designed to be 3 stages. Miller capacitor and current source bias are both designed to be 3 stages. High GBW with large current for high curcuit performance and low GBW with small current for enough performance and low power.

4.2 Voltage detector

This voltage detector is for AGC system. Comparator of this voltage detector is shown in Fig. 5. The current is based on a rail-to-rail structure to get a high dynamic range. For the specific use of this receiver, the voltage detector can supply a detection range of 128mV to 896mV with a step of 12mV for 64 steps.

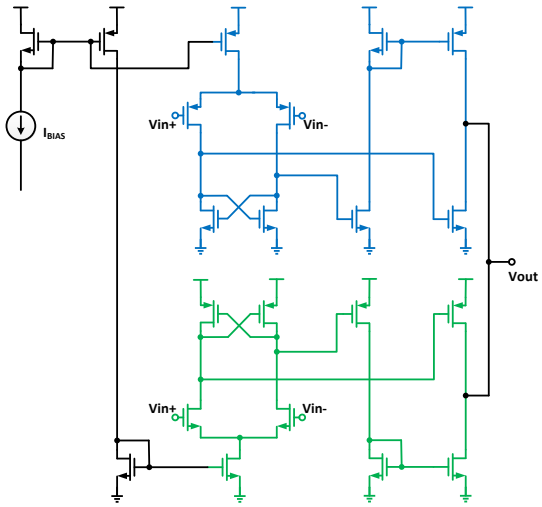


Fig. 5 Circuit schematics of the rail-to-rail comparator

5. Layout and Simulation Results

5.1 Layout

Layout of TI-LPF and voltage detector using 65nm CMOS process is shown in Fig. 6. Symmetry principle and dummy matching are used for decreasing mismatch. The simulation results is come from Cadence Virtuoso.

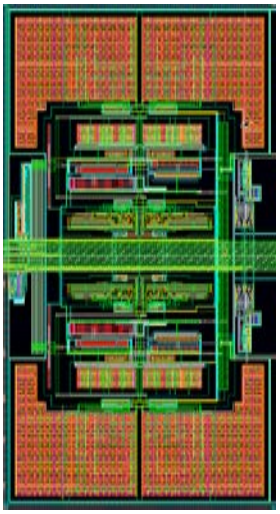


Fig. 6 Layout of TI-LPF and voltage detector

5.2 Simulation result of Amp

Amp's simulation is under the condition of 1.2V supply voltage and 715mV common mode voltage. Gain and frequency responses is shown in Fig. 7.

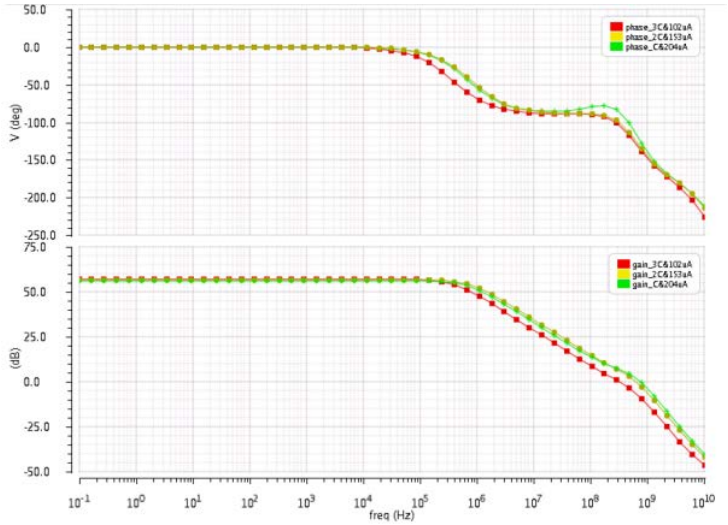


Fig. 7 Gain and frequency responses of TI-LPF's Amp

More details are shown in Table 1.

Table 1 More simulation results of TI-LPF's Amp

Configuration Mode		Mode 1	Mode 2	Mode 3
Miller Capacitance Cc		3C	2C	C
Current (uA)		102	153	204
Gain (dB)		56.973	56.503	55.883
Power (mW)		3.187	4.633	6.002
Phase Margin (°)		65.2	61.6	57.1
Bandwidth (kHz)		523.2	756.5	1386
GBW (MHz)		369.2	505.8	862.8
Slew Rate (V/us)		UP:163.9 DN:127.0	UP:234.9 DN:170.9	UP:374.9 DN:255.2
Equivalent Input Noise (V^2)		3.63e-11 [0-3MHz]	6.94e-11 [0-10MHz]	1.15e-10 [0-20MHz]
CMFB	Gain (dB)	52.42		
	Phase Margin (°)	76.38	71.45	61.66

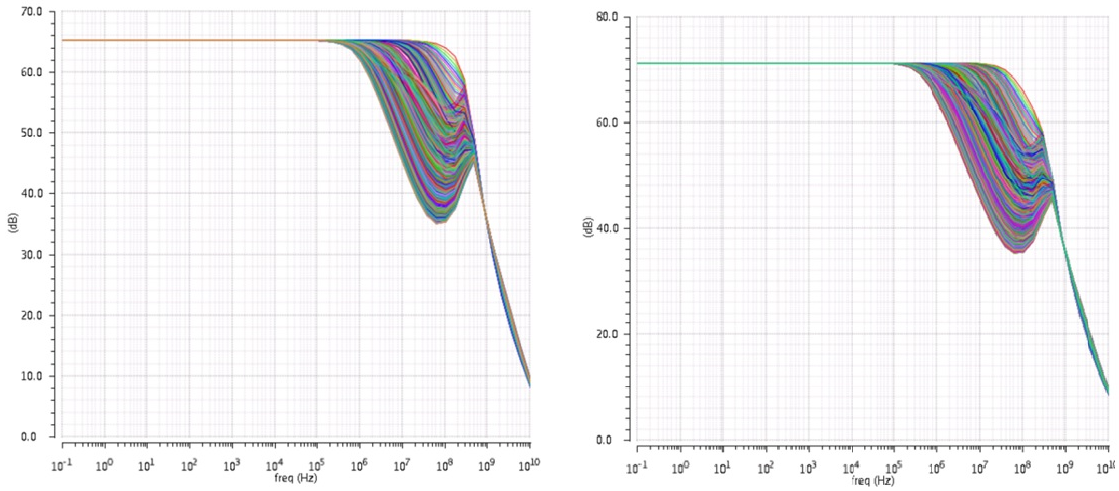
Different configuration modes (shown in Table 2) are for different signal bandwidth.

Table 2 Configuration modes

Miller Capacitance Cc	GBW (MHz)	Bandwidth (BW)
3C	369.2	$BW \leq 3.5MHz$
2C	505.8	$3.5MHz \leq BW \leq 8.5MHz$
C	862.8	$8.5MHz \leq BW$

5.2 Simulation result of TI-LPF

The simulation is under the condition of 1.2V supply voltage and 715mV common mode voltage. Configuration of 71.2dBΩ and 65.1dBΩ trans-impedance gain responses is shown in Fig. 8. The tunable range of TI-LPF's bandwidth is 0.5MHz to 64.06MHz at 71.2dBΩ trans-impedance and 0.989MHz to 185.5MHz at 65.1dBΩ trans-impedance.



(a) (b)

Fig. 8 Trans-impedance gain responses of TI-LPF (a) 65.1dBΩ (b) 71.2dBΩ

6. Conclusion

This paper reports an active RC trans-impedance low pass filter (TI-LPF) with variable gain and bandwidth that can be used in 200MHz to 6GHz zero-IF software-defined radio (SDR) receivers. In this paper, we put forward a point of view that in the TI-LPF structure we presented, it's better to design the GBW of this TI-LPF's amplifier 10 times of signal frequency. The simulation results present that this TI-LPF exhibits 64x bandwidth tunability (1MHz to 64MHz), 3 stages of trans-impedance gain of 71.2dBΩ, 67.6dBΩ and 65.1dBΩ, a static power dissipation less than 6.002mW, and a total summarized noise less than 5.969 x $10^{-15}V^2$.

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